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EXAMINER	
PRABHAKHER, PRITHAM DAVID	
ART UNIT	PAPER NUMBER
2622	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,860	WU, YUNG-CHUAN	
	Examiner	Art Unit	
	Pritham Prabhakher	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwai (US Patent No.: 6204910B1).

In regard to ***Claim 1****, Iwai teaches of a charge-coupled device (CCD) sensing apparatus, comprising:*

a first photo sensor set with a plurality of first photo sensors for receiving a light signal and generating a plurality of corresponding first charge signals (The first photo sensor set is considered to be the leftmost light receiving elements (photodiodes) that receive light and generate even and odd (plurality) electrical signals, ***Column 4, Lines 16 et seq. and Figure 2****); and*

a first CCD shift register (Made up of CCD Analog Shift Registers 111 and 112) including a first CCD component set (CCD Analog Shift Register 111) and a second CCD component set (CCD Analog Shift Register 112), wherein the first CCD component set can receive a first part of the first charge signals (The CCD Analog Shift Register 111 receives the odd component signals from the leftmost light receiving elements, ***Column 4, Lines 46-49****); the first part of the first charge signals are then*

sequentially output from the first CCD component set to a first charge storage component (The odd component signals are sequentially transferred and output through the CCD Analog Shift Register 111 to the Output Buffer 121 (First Charge Storage Component), ***Column 4, Lines 46-48 and Figure 2)*** *and then converted to corresponding voltages; the second CCD component set can receive the remaining part of the first charge signals (The CCD Analog Shift Register 112 receives the even component signals from the leftmost light receiving elements,* ***Column 4, Lines 49-51)*** *; and the remaining part of the first charge signals are then sequentially output from the second CCD component set to a second charge storage component (The even component signals are sequentially transferred and output through the CCD Analog Shift Register 112 to the Output Buffer 122 (Second Charge Storage Component),* ***Column 4, Lines 49-51 and Figure 2)*** *and then converted to corresponding voltages.*

Although Iwai does not specifically teach of converting the signals to corresponding voltages, Figure 3 shows that ADC converters 133 and 134 are present for using the voltages output from the amplifiers and a reference voltage to convert the data into digital data. Official notice is taken saying that it would have been obvious at the time of the invention to use an ADC converter that compared voltages (from the amplifier) before the conversion to digital data because it provides processing flexibility and higher signal to noise ratio during transmission to reduce error rates.

With regard to ***Claim 2****, Iwai teaches of the CCD sensing apparatus according to claim 1, wherein the first photo sensors are of the same size, and also are spaced at the same intervals (It is inherent that the photosensors are of the same size and are spaced*

at the same intervals because when the even and odd signals are generated they have to be done so symmetrically).

In regard to ***Claim 3****, Iwai teaches of the CCD sensing apparatus according to claim 1, wherein the first CCD component set and the second CCD component set are electrically isolated (Figure 2 shows that the first CCD component set (111) and the second CCD component set (112) are electrically isolated).*

Regarding ***Claim 4****, Iwai teaches of the CCD sensing apparatus according to claim 1, wherein the first CCD component set includes the same number of CCD components as the second CCD component set (It is inherent that the first CCD component set 111 includes the same number of components as the second CCD component set 112, because the even and odd signal components have to be sequentially transferred symmetrically).*

With regard to ***Claim 5****, Iwai teaches of the CCD sensing apparatus according to claim 1, further comprising:*

a second photo sensor set with a plurality of second photo sensors for receiving a light signal and generating a plurality of corresponding second charge signals (The second photo sensor set is considered to be the rightmost light receiving elements (photodiodes) that receive light and generate even and odd (plurality) electrical signals (second charge signals), ***Column 4, Lines 16 et seq. and Figure 2)****, wherein the second photo sensor set and the first photo sensor set are arranged in a staggered-type configuration (Figure 2 shows that the first photo sensor set is on the far left starting at S1 and the second set of photo sensors starts at S7500); and*

a second CCD shift register (Made up of CCD Analog Shift Registers 113 and 114) including a third CCD component set (CCD Analog Shift Register 113) and a fourth CCD component set (CCD Analog Shift Register 114), wherein the third CCD component set can receive a part of the second charge signals (The CCD Analog Shift Register 113 receives the odd component signals from the rightmost light receiving elements, ***Column 4, Lines 51-57)****; the second charge signals are then sequentially output from the third CCD component set to a third charge storage component (The odd component signals are sequentially transferred and output through the CCD Analog Shift Register 113 to the Output Buffer 123 (Third Charge Storage Component),* ***Column 4, Lines 51-57 and Figure 2)*** *and then converted to corresponding voltages; the fourth CCD component set can receive the remaining part of the second charge signals (The CCD Analog Shift Register 114 receives the even component signals from the rightmost light receiving elements,* ***Column 4, Lines 51-57)****; and the remaining part of the second charge signals are then sequentially output from the fourth CCD components set to a fourth charge storage component (The even component signals are sequentially transferred and output through the CCD Analog Shift Register 114 to the Output Buffer 124 (Fourth Charge Storage Component),* ***Column 4, Lines 51-57 and Figure 2)*** *and then converted to corresponding voltages.*

Again, Iwai does not specifically teach of converting the signals to corresponding voltages, Figure 3 shows that ADC converters 133 and 134 are present for using the voltages output from the amplifiers and a reference voltage to convert the data into digital data. Official notice is taken saying that it would have been obvious at the time of

the invention to use an ADC converter that compared voltages (from the amplifier) before the conversion to digital data because it provides processing flexibility and higher signal to noise ratio during transmission to reduce error rates.

*Regarding **Claim 6**, Iwai teaches of the CCD sensing apparatus according to claim 5, wherein the second photo sensors are of the same size as the first photo sensors, and also are spaced at the same interval as the first photo sensors (It is inherent that the photosensors are of the same size and are spaced at the same intervals because when the even and odd signals are generated they have to be done so symmetrically. Figure 3 shows that the even signals are multiplexed together and the odd signals are multiplexed together. Therefore, symmetry must inherently exist.)*

*With regard to **Claim 7**, Iwai teaches of the CCD sensing apparatus according to claim 1, wherein the CCD sensing apparatus is used in a scanner (The CCD sensing apparatus is used in a scanner 4, **See Figure 1 and Column 4, Line 7)**.*

*In regard to **Claim 8**, Iwai teaches of a charge-coupled device (CCD) sensing apparatus, comprising:*

*a first photo sensor set with a plurality of first photo sensors for receiving a light signal and generating a plurality of corresponding first charge signals (The first photo sensor set is considered to be the leftmost and rightmost light receiving elements (photodiodes) that receive light and generate even and odd (plurality) electrical signals, **Column 4, Lines 16 et seq. and Figure 2)**; and*

a first CCD shift register (Made up of CCD Analog Shift Registers 111 and 113) including a first CCD component set (CCD Analog Shift Register 111) and a second CCD component set (CCD Analog Shift Register 113), wherein the first CCD component set can receive a first part of the first charge signals (The CCD Analog Shift Register 111 receives the odd component signals from the leftmost light receiving elements, ***Column 4, Lines 46-49)****; the first part of the first charge signals are then sequentially output from the first CCD component set to a first charge storage component (The odd component signals are sequentially transferred and output through the CCD Analog Shift Register 111 to the Output Buffer 121 (First Charge Storage Component),* ***Column 4, Lines 46-48 and Figure 2)*** *and then converted to corresponding voltages; the second CCD component set can receive a second part of the first charge signals (The CCD Analog Shift Register 113 receives the odd component signals from the rightmost light receiving elements,* ***Column 4, Lines 51-57)*** *; and the second part of the first charge signals are then sequentially output from the second CCD component set to a second charge storage component (The odd component signals are sequentially transferred and output through the CCD Analog Shift Register 113 to the Output Buffer 123 (Second Charge Storage Component),* ***Column 4, Lines 51-57 and Figure 2)*** *and then converted to corresponding voltages.*

a second CCD shift register (Made up of CCD Analog Shift Registers 112 and 114), wherein the first CCD shift register and the second CCD shift register are located on opposite sides of the first photo sensor set (The first photo sensor set consists of the photodiodes located in the center between Shift Gates 1 and 2 as shown in Figure 2.

The first shift register is made up of CCD Analog shift registers 111 and 113. The second shift register is made up of CCD Analog shift registers 112 and 114. Looking at Figure 2, it is shown that the first and second shift registers are located on opposite sides of the first photo sensor); the second CCD shift register includes a third CCD component set (CCD Analog Shift Register 112) and a fourth CCD component set (CCD Analog Shift Register 114); the third CCD component set can receive a third part of the first charge signals (The CCD Analog Shift Register 112 receives the even component signals from the leftmost side of the photodiodes (third part of the first charge signals), ***Column 4, Lines 45-50)*** *; the third part of the first charge signals are then sequentially output from the third CCD component set to a third charge storage component (The signals from the third part of the first charge signal are then sequentially output from the third CCD component 112 to an Output Buffer 122 (third charge storage component),* ***Column 4, Lines 45-50 and Figure 2)*** *and then converted to corresponding voltages; the fourth CCD component set can receive the remaining part of the first charge signals (CCD analog shift register 114 receives the even component signals from the rightmost side of the photodiodes (fourth part of the first charge signals),* ***Column 4, Lines 51-57)****; and the remaining part of the first charge signals are then sequentially output from the fourth CCD component set to a fourth charge storage component (The signals from the fourth part of the first charge signal are then sequentially output from the fourth CCD component 114 to an Output Buffer 124 (fourth charge storage component),* ***Column 4, Lines 51-57 and Figure 2)*** *and then converted to corresponding voltages.*

Although Iwai does not specifically teach of converting the signals to corresponding voltages, Figure 3 shows that ADC converters 133 and 134 are present for using the voltages output from the amplifiers and a reference voltage to convert the data into digital data. Official notice is taken saying that it would have been obvious at the time of the invention to use an ADC converter that compared voltages (from the amplifier) before the conversion to digital data because it provides processing flexibility and higher signal to noise ratio during transmission to reduce error rates.

Claims 9-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwai (US Patent No.: 6204910B1) and further in view of Harada (US Pub No.: 2002/0071046A1).

*Regarding **Claim 9**, Iwai teaches of a charge-coupled device (CCD) sensing apparatus, comprising:*

*a first photo sensor set having a plurality of first photo sensors for receiving a light signal and generating a plurality of corresponding first charge signals (The first photo sensor set is considered to be the leftmost light receiving elements (photodiodes) that receive light and generate even and odd (plurality) electrical signals, **Column 4, Lines 16 et seq. and Figure 2**); and*

a first CCD shift register (Made up of CCD Analog Shift Registers 111 and 112) comprising P CCD component sets, where P is a positive integer greater than 2 (A first

component set (CCD Analog Shift Register 111) and a second CCD component set (CCD Analog Shift Register 112) make up the entire first CCD shift register), wherein each of the P CCD component sets is coupled to corresponding first charge storage components (Each of the CCD components 111 and 112 are coupled to output buffers (charge storage components) 121 and 122 respectively, ***Figure 2)****; each of the P CCD component sets can receive part of the first charge signals (The CCD Analog Shift Register 111 receives the odd component signals from the leftmost light receiving elements,* ***Column 4, Lines 46-49.*** *The CCD Analog Shift Register 112 receives the even component signals from the leftmost light receiving elements,* ***Column 4, Lines 49-51)****, the charge signals are then sequentially output from each of the P CCD component sets to the corresponding first charge storage components (The odd component signals are sequentially transferred and output through the CCD Analog Shift Register 111 to the Output Buffer 121 (First Charge Storage Component),* ***Column 4, Lines 46-48 and Figure 2.*** *The even component signals are sequentially transferred and output through the CCD Analog Shift Register 112 to the Output Buffer 122 (Second Charge Storage Component),* ***Column 4, Lines 49-51 and Figure 2)*** *and then converted to corresponding voltages.*

Although Iwai does not specifically teach of converting the signals to corresponding voltages, Figure 3 shows that ADC converters 133 and 134 are present for using the voltages output from the amplifiers and a reference voltage to convert the data into digital data. Official notice is taken saying that it would have been obvious at the time of the invention to use an ADC converter that compared voltages (from the

amplifier) before the conversion to digital data because it provides processing flexibility and higher signal to noise ratio during transmission to reduce error rates.

Also, although Iwai teaches of 2 CCD components for the first shift register, it is not explicitly taught that there are more than 2 CCD components present (P). Harada teaches of more than one CCD component being present (14A –14C) in Figure 5 and ***Paragraph 0064 of Harada****. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate into the teachings of Iwai the ability to have more than 2 CCD components present because can make the screen of the CCD image apparatus larger, make the apparatus have a higher resolution and make the apparatus have a higher speed,* ***Paragraph 0071 of Harada****.*

With regard to ***Claim 10,*** *Iwai and Harada disclose the CCD sensing apparatus, according to claim 9, wherein the first photo sensors are of the same size, and also are spaced at the same interval* ***(****It is inherent that the photosensors are of the same size and are spaced at the same intervals because when the even and odd signals are generated they have to be done so symmetrically****)****.*

In regard to ***Claim 11****, Iwai and Harada disclose the CCD sensing apparatus according to claim 9, wherein the P CCD component sets are electrically isolated from each other* ***(****Figure 2 of Iwai shows that the first CCD component set (111) and the second CCD component set (112) are electrically isolated****)****.*

Regarding ***Claim 12****, Iwai and Harada disclose the CCD sensing apparatus according to claim 9, wherein each of the P CCD component sets includes the same number of CCD components* ***(****It is inherent that the first CCD component set 111*

includes the same number of components as the second CCD component set 112, because the even and odd signal components have to be sequentially transferred symmetrically).

With regard to ***Claim 13****, Iwai and Harada disclose the CCD sensing apparatus according to claim 9, further comprising:*

a second photo sensor set having a plurality of second photo sensors for receiving a light signal and generating a plurality of corresponding second charge signals (The second photo sensor set is considered to be the rightmost light receiving elements that receive light and generate even and odd (plurality) electrical signals (second charge signals), ***Column 4, Lines 16 et seq. and Figure 2 of Iwai)****, wherein the second photo sensor set and the first photo sensor set are arranged in a staggered-type configuration (Figure 2 of Iwai shows that the first photo sensor set is on the far left starting at S1 and the second set of photo sensors starts at S7500); and*

a second CCD shift register (Made up of CCD Analog Shift Registers 113 and 114) including Q CCD component sets, where Q is a positive integer greater than 2, wherein each of the Q CCD component sets is coupled to a second charge storage component; each of the Q CCD component sets can receive part of the second charge signals; and the charge signals are then sequentially output from each of the Q CCD component sets to the corresponding second charge storage component (The CCD Analog Shift Register 113 receives the odd component signals from the rightmost light receiving elements. The odd component signals are sequentially transferred and output through the CCD Analog Shift Register 113 to the Output Buffer 123 (Third Charge

Storage Component). The CCD Analog Shift Register 114 receives the even component signals from the rightmost light receiving elements. The even component signals are sequentially transferred and output through the CCD Analog Shift Register 114 to the Output Buffer 124 (Fourth Charge Storage Component), ***Column 4, Lines 51-57 and Figure 2 of Iwai)*** *and then converted to corresponding voltages.*

Again, Iwai does not specifically teach of converting the signals to corresponding voltages, Figure 3 shows that ADC converters 133 and 134 are present for using the voltages output from the amplifiers and a reference voltage to convert the data into digital data. Official notice is taken saying that it would have been obvious at the time of the invention to use an ADC converter that compared voltages (from the amplifier) before the conversion to digital data because it provides processing flexibility and higher signal to noise ratio during transmission to reduce error rates.

Also, although Iwai teaches of 2 CCD components corresponding to the second shift register, it is not explicitly taught that there are more than 2 CCD components present (Q). Harada teaches of more than one CCD component being present (14D – 14F) in Figure 5 and ***Paragraph 0064 of Harada****. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate into the teachings of Iwai the ability to have more than 2 CCD components present because this can make the screen of the CCD image apparatus larger, make the apparatus have a higher resolution and make the apparatus have a higher speed,* ***Paragraph 0071 of Harada****.*

Regarding ***Claim 14****, Iwai and Harada disclose the CCD sensing apparatus according to claim 13, wherein the second photo sensors are of the same size as the*

first photo sensors, and are also spaced at the same interval as the first photo sensors (It is inherent that the photosensors are of the same size and are spaced at the same intervals because when the even and odd signals are generated they have to be done so symmetrically. Figure 3 shows that the even signals are multiplexed together and the odd signals are multiplexed together. Therefore, symmetry must inherently exist.)

With regard to ***Claim 15****, Iwai and Harada disclose the CCD sensing apparatus according to claim 9, wherein the CCD sensing apparatus is used in a scanner (The CCD sensing apparatus is used in a scanner 4,* ***See Figure 1 and Column 4, Line 7 of Iwai)****.*

In regard to ***Claim 16****, Iwai teaches of a charge-coupled device (CCD) sensing apparatus, comprising:*

a first photo sensor set having a plurality of first photo sensors for receiving a light signal and generating a plurality of corresponding first charge signals (The first photo sensor set is considered to be the leftmost and rightmost light receiving elements (photodiodes) that receive light and generate even and odd (plurality) electrical signals, ***Column 4, Lines 16 et seq. and Figure 2)****; and*

a first CCD shift register (Made up of CCD Analog Shift Registers 111 and ***113)*** *comprising P CCD component sets (CCD Analog Shift Registers 111 and 113), where P is a positive integer greater than 2, wherein each of the P CCD component sets is coupled to corresponding first charge storage components (The odd component signals are sequentially transferred and output through the CCD Analog Shift Register 111 to*

the Output Buffer 121 and through the CCD Analog Shift Register 113 to the Output Buffer 123 (First Charge Storage Components), ***Column 4, Lines 48-57 and Figure 2);***

a second CCD shift register (Made up of CCD Analog Shift Registers 112 and 114), wherein the first CCD shift register and the second CCD shift register are located on opposite sides of the first photo sensor set (The first photo sensor set consists of the photodiodes located in the center between Shift Gates 1 and 2 as shown in Figure 2. The first shift register is made up of CCD Analog shift registers 111 and 113. The second shift register is made up of CCD Analog shift registers 112 and 114. Looking at Figure 2, it is shown that the first and second shift registers are located on opposite sides of the first photo sensor); the second CCD shift register comprises Q CCD component sets (CCD Analog Shift Registers 112 and 114), where Q is a positive integer greater than 2; each of the Q CCD component sets is coupled to second charge storage components (Even component signals are output sequentially from the CCD Analog Shift Register 112 to an Output Buffer 122, and from the CCD Analog Shift Register 114 to an Output Buffer 124. Output buffers 122 and 124 form the second charge storage components, ***Column 4, Lines 45-57 and Figure 2 of Iwai);***

each of the P CCD component sets and Q CCD component sets can receive part of the first charge signals (The CCD Analog Shift Registers 111 and 113 receive odd component signals from the leftmost and rightmost light receiving elements respectively (P CCD Components). The CCD Analog Shift Registers 112 and 114 receive even component signals from the leftmost and rightmost light receiving elements respectively (Q CCD Components), ***Column 4, Lines 45-57 of Iwai);*** *and the*

charge signals are then sequentially output from each of the P CCD component sets and Q CCD component sets to the corresponding first charge storage components and the corresponding second charge storage components (The odd component signals are sequentially transferred and output through the CCD Analog Shift Registers 111 and 113 to the Output Buffers 121 and 123 respectively. The even component signals are sequentially transferred and output through the CCD Analog Shift Registers 112 and 114 to the Output Buffers 122 and 124 respectively, ***Column 4, Lines 45-57 and Figure 2 of Iwai)*** *and then converted to corresponding voltages accordingly.*

However, Iwai does not specifically teach of converting the signals to corresponding voltages, but Figure 3 shows that ADC converters 133 and 134 are present for using the voltages output from the amplifiers and a reference voltage to convert the data into digital data. Official notice is taken saying that it would have been obvious at the time of the invention to use an ADC converter that compared voltages (from the amplifier) before the conversion to digital data because it provides processing flexibility and higher signal to noise ratio during transmission to reduce error rates.

Also, although Iwai teaches of 2 CCD components corresponding to the first and second shift registers each, it is not explicitly taught that there are more than 2 CCD components present for the first shift register (P) and the second shift register (Q). Harada teaches of more than one CCD component being present (14A –14F) in Figure 5 and ***Paragraph 0064 of Harada****. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate into the teachings of Iwai the ability to have more than 2 CCD components present because this can make the screen of the*

CCD image apparatus larger, make the apparatus have a higher resolution and make the apparatus have a higher speed, ***Paragraph 0071 of Harada****.*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pritham Prabhakher whose telephone number is 571-270-1128. The examiner can normally be reached on M-F (7:30-5:00) Alt Friday's Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571)272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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